WHAT IS CLAIMED IS:

1. A method of forming a fin field effect transistor, comprising:

forming a fin;

forming a source region adjacent a first end of the fin and a drain region adjacent a second end of the fin;

forming a dummy gate comprising a first material in a first pattern over the fin;

forming a dielectric layer adjacent sides of the dummy gate;

removing the first material to form a trench in the dielectric layer corresponding to the first pattern; and

forming a metal gate in the trench.

2. The method of claim 1, wherein the metal gate contacts at least three surfaces of the fin.

3. The method of claim 2, wherein the fin field effect transistor comprises a tri-gate fin field effect transistor.

4. The method of claim 1, wherein the dielectric layer comprises tetraethylorthosilicate.

5. The method of claim 1, further comprising:

forming a gate insulation layer in the trench prior to forming the metal gate.

6. The method of claim 5, wherein the gate insulation layer comprises at least one of SiO, $SiO_2$, SiN, SiON, $HFO_2$, $ZrO_2$, $Al_2O_3$, HFSiO(x) ZnS, and $MgF_2$.

7. The method of claim 1, wherein the first crystalline material comprises polysilicon.

8. The method of claim 1, further comprising:

forming a dummy oxide layer over the fin prior to forming the dummy gate.

9. The method of claim 8, wherein forming the dummy gate comprises:

depositing a layer of the first material over the fin; and

etching the layer of the first material to form the dummy gate in the first pattern.

10. The method of claim 1, wherein forming the metal gate comprises:

depositing a metal material to fill the trench.

11. A tri-gate fin field effect transistor, comprising:

a fin comprising a plurality of surfaces and having a source region and a drain region formed adjacent each end of the fin; and

a metal gate formed on three surfaces of the plurality of surfaces.

12. The fin field effect transistor of claim 11, further comprising:

a gate insulation layer formed between the metal gate and the fin.

13. The fin field effect transistor of claim 12, further comprising:

a dielectric layer formed adjacent the metal gate and formed over the fin, source region and drain region.

14. The fin field effect transistor of claim 12, wherein the gate insulation layer comprises at least one of SiO, $SiO_2$, SiN, SiON, $HFO_2$, $ZrO_2$, $Al_2O_3$, HFSiO(x) ZnS, and $MgF_2$.

15. The fin field effect transistor of claim 11, wherein the fin has a width ranging from about 100 Å to about 500 Å.

16. A method of forming a fin field effect transistor, comprising:

forming a fin;

forming a source region adjacent a first end of the fin and a drain region adjacent a second end of the fin;

forming a dummy oxide layer over the fin;

depositing a layer of first material over the fin and dummy oxide layer;

etching the layer of the first material to form a dummy gate in a first pattern;

depositing a dielectric layer over the dummy gate and source and drain regions;

planarizing the dielectric layer to expose a top surface of the dummy gate;

removing the first material to form a trench in the dielectric layer corresponding to the first pattern;

forming a gate insulation layer in the trench; and

forming a metal gate in the trench.

17. The method of claim 16, wherein the metal gate contacts at least three surfaces of the fin.

18. The method of claim 16, wherein the fin field effect transistor comprises a tri-gate fin field effect transistor.

19. The method of claim 16, wherein the dielectric layer comprises tetraethylorthosilicate.

20. The method of claim 16, wherein the first material comprises polysilicon.